Clean copy of allowed claims

8. A computer implemented method for simulating an anti-resonance circuit of a section of a microprocessor, comprising:

simulating a load of the anti-resonance circuit;

simulating using a simulated transistor model, at least one high frequency capacitance of the anti-resonance circuit in parallel with the simulated load; and

simulating using a simulated capacitor model, an intrinsic capacitance of the section of the microprocessor in parallel with the simulated load.

9. The method of claim 8, wherein the load is simulated with a simulated resistor.

10. The method of claim 9, wherein the simulated resistor is a simulated voltage controlled resistor.

11. The method of claim 8, wherein simulation of the anti-resonance circuit is synchronized with a simulated clock cycle.

13. The method of claim 11, wherein simulation of the anti-resonance circuit begins on a leading edge of the simulated clock cycle.